# CLAIMS

What is claimed is:

1. A mask comprising a pattern to modify a circuitry feature exposed in a radiation sensitive layer by transmitting modifying radiation according to the pattern to a region of the radiation sensitive layer containing the circuitry feature.

2. The mask of claim 1:

wherein the circuitry feature includes a corner rounded portion; and

wherein the pattern includes a radiation opaque portion corresponding to the circuitry feature having a corner cutout corresponding to the corner rounded portion reduce the corner rounded portion by exposing the corner rounded portion with radiation transmitted through the corner cutout region.

3. The mask of claim 1, wherein the pattern comprises a radiation intensity reducer to create the modifying radiation by reducing a portion of incident radiation provided to the mask and transmitting the modifying radiation to the region containing the circuitry feature.

4. The mask of claim 1, wherein the radiation intensity reducer comprises a plurality of proximate opaque subresolution features to reduce a portion of incident radiation that is provided to the subresolution features.

5. The mask of claim 1, wherein the radiation intensity reducer comprises an applied phase shifting material that prevents a portion of radiation provided to the mask from exposing the radiation sensitive layer.

6. The mask of claim 1, wherein the pattern comprises a proximity effect distortion reducing feature selected from the group consisting of a serif to reduce corner rounding by emphasizing a corner of the circuitry feature and a hammerhead to reduce line shortening by emphasizing an end of the circuitry feature.

7. The mask of claim 1, wherein the pattern comprises a phase shifter.

8. The mask of claim 1:

wherein the circuitry feature includes a line segment having a pattern shift distortion that shifts the line segment to a first side of the line segment; and

wherein the pattern comprises a high radiation transmittance region corresponding to the first side of the line segment and a low radiation transmittance region corresponding to an opposite side of the line segment to reduce the pattern shift distortion by providing more of the modifying radiation to the high transmittance region than the low transmittance region.

9. The mask of claim 1, wherein the pattern further comprises:

an opaque portion to block a portion of radiation incident to the mask from exposing the circuitry feature; and

a transparent portion to transmit modifying radiation to the circuitry feature.

10. The mask of claim 1:

wherein the exposed circuitry feature comprises a linewidth; and

wherein the pattern is a pattern to reduce the linewidth by transmitting linewidth reducing radiation to the region containing the linewidth.

11. The mask of claim 1, wherein the pattern is a pattern to reduce a proximity effect distortion in the exposed circuitry feature by transmitting proximity effect reducing radiation to the region containing the circuitry feature.

12. A semiconductor device created by using a first mask having a first pattern to expose a first feature in a radiation sensitive layer and using a second mask having a second pattern to modify the first feature by providing modifying radiation to a region of the radiation sensitive layer containing the first feature.

13. The semiconductor device of claim 12, further created by using the second mask having a second pattern to reduce a proximity effect distortion of the first feature.

14. The semiconductor device of claim 12, comprising at least a portion of a processor to execute instructions.

15. The semiconductor device of claim 12:

further creating by using the first mask having a first pattern to expose a gate feature having a corner rounded region; and

further created by using the second mask having a second pattern to modify a size and a shape of the gate feature by providing modifying radiation to the region containing the gate feature.

16. The semiconductor device of claim 12:

further creating by using the first mask having a first pattern to expose a gate feature having a corner rounded region; and

further created by using the second mask having a second pattern having a transparent portion to reduce the corner rounded region of the gate feature by providing modifying radiation to the corner rounded region.

17. The semiconductor device of claim 12, further created by using the second mask having a second pattern comprising a pattern portion selected from the group consisting of: a phase shifter, a plurality of proximate subresolution features, and a layer of material to reduce radiation transmittance substantially more than quartz.

18. A second mask having a second pattern that corresponds to a first pattern of a first mask, the first pattern to expose an exposure feature in a radiation sensitive layer, the second pattern comprising a transparent portion to reduce a proximity effect distortion of the exposure feature by providing modifying radiation to a region of the radiation sensitive layer that contains the exposure feature.

19. The second mask of claim 18:

wherein the exposure feature comprises a gate feature having a corner rounded region; and

wherein the transparent portion comprises a cutout portion sufficiently proximate to the corner rounded region to reduce the corner rounded region by providing radiation to the corner rounded region.

20. The second mask of claim 18, further comprising a pattern portion selected from the group consisting of: a phase shifter, a plurality of proximate subresolution features, and a layer of radiation reducing material to transmit substantially less radiation than a region of quartz of the mask.

21. A method comprising:

creating a circuitry feature in a radiation sensitive layer coupled with a wafer during a first exposure by transmitting radiation to the layer through a first mask having a first circuitry pattern; and

modifying the circuitry feature during a second exposure by transmitting modifying radiation to the layer through a second mask having a second circuitry pattern and a transparent portion corresponding to a region of the layer containing the circuitry feature.

22. The method of claim 21, wherein modifying includes reducing a subwavelength distortion of the circuitry feature.

23. The method of claim 21, wherein modifying includes reducing a proximity effect distortion of the circuitry feature.

24. An integrated circuit created by the method of claim 23.